Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Canceled)

2. (Currently Amended) The transceiver of claim [[1]] 4, wherein said bus is configured to have a ring shape.

3. (Currently Amended) The transceiver of claim [[1]] 4, wherein said bus is configured to have a ring shape around a logic core.

4. (Previously Presented) A transceiver, comprising:

multiple parallel ports;

multiple serial ports;

a bus connecting said multiple parallel ports and said multiple serial ports on a common substrate with said multiple parallel ports and said multiple serial ports; and

a packet bit error rate tester (BERT) connected to said bus, said packet BERT able to determine bit error rates of at least one of said multiple parallel ports and said multiple serial ports.

5. (Previously Presented) A transceiver, comprising:

multiple parallel ports;

multiple serial ports; and

a bus connecting said multiple parallel ports and said multiple serial ports on a common substrate with said multiple parallel ports and said multiple serial ports;

wherein said multiple parallel ports include two parallel ports and said multiple serial ports includes four serial ports.

6. (Previously Presented) A transceiver, comprising:

multiple parallel ports;

multiple serial ports; and

a bus connecting said multiple parallel ports and said multiple serial ports on a common substrate with said multiple parallel ports and said multiple serial ports;

wherein said multiple parallel ports are XGMII parallel ports.

7. (Previously Presented) A transceiver, comprising:

multiple parallel ports;

multiple serial ports; and

a bus connecting said multiple parallel ports and said multiple serial ports on a common substrate with said multiple parallel ports and said multiple serial ports;

wherein said multiple serial ports are XAUI serial ports.

8. (Previously Presented) A transceiver, comprising:

multiple parallel ports;

multiple serial ports; and

a bus connecting said multiple parallel ports and said multiple serial ports on a common substrate with said multiple parallel ports and said multiple serial ports;

wherein said serial ports convert between a XAUI serial protocol and a XGMII parallel protocol using a XGXS conversion protocol.

9. (Currently Amended) The transceiver of claim [[1]] 4, wherein said bus is a parallel bus.

10. (Previously Presented) A transceiver, comprising:

multiple parallel ports;

multiple serial ports; and

a parallel bus connecting said multiple parallel ports and said multiple serial ports on a common substrate with said multiple parallel ports and said multiple serial ports;

wherein said parallel bus includes multiple transmission lines having a common path length.

11. (Original) The transceiver of claim 9, wherein each of said serial ports include a serial-to-parallel converter, a parallel port of said serial-to-parallel converter connected to said parallel bus.

12. (Previously Presented) A transceiver, comprising:

multiple parallel ports;

multiple serial ports;

a bus connecting said multiple parallel ports and said multiple serial ports on a common substrate with said multiple parallel ports and said multiple serial ports; and

at least one management pad, said management pad able to determine data protocols and electricals for said transceiver.

13. (Original) The transceiver of claim 12, wherein said management pad is responsive to two or more protocols.

14. (Original) The transceiver of claim 13, wherein said two or more protocols include an IEEE Std 802.3 clause 22 management standard and an IEEE Std 802.3 clause 45 management standard.

15. (Original) The transceiver of claim 12, wherein said management pad is responsive to a data protocol of a first type of standard, and an electrical protocol of a second type of standard.

16. (Original) The transceiver of claim 15, wherein said first type of standard is one of an IEEE Std 802.3 clause 45 standard and an IEEE Std 802.3 clause 22 standard, and said second type of standard is the other of said IEEE Std 802.3 clause 45 standard and said IEEE Std 802.3 clause 22 standard.

17. (Currently Amended) The transceiver of claim [[1]] 10, wherein data clock rates of said multiple serial [[data]] ports and said multiple parallel [[data]] ports are programmable.

18. (Canceled)

19. (Currently Amended) The transceiver of claim [[1]] 10, wherein two of said multiple serial [[data]] ports are enabled.

20. (Original) The transceiver of claim 19, wherein at least one of said multiple serial ports is disabled.

21. (Currently Amended) The transceiver of claim [[1]] 10, wherein at least one of said multiple parallel ports is enabled.

22. (Original) The transceiver of claim 21, wherein at least one of said multiple parallel ports is disabled.

23. (Currently Amended) The transceiver of claim [[1]] 4, further comprising at least one custom logic block connected to said bus.

24. (Currently Amended) The transceiver of claim [[1]] 10, further comprising a configuration block that enables and disables said multiple parallel ports and said multiple serial ports to configure said transceiver.

25. (Canceled)